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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) 8734.232.00/US	
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Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

applicant/inventor.
 assignee of record of the entire interest.
 See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
 (Form PTO/SB/96)
 attorney or agent of record.
 Registration number 53,005
 attorney or agent acting under 37 CFR 1.34.
 Registration number if acting under 37 CFR 1.34 _____.

/Valerie P. Hayes/

Signature

Valerie P. Hayes

Typed or printed name

202 - 496 - 7500

Telephone number

August 1, 2011

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
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Docket No.: 8734.232 US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
KIM, Seok Su

Application No.: 10/664,912

Filed: September 22, 2003

For: **DATA DRIVING APPARATUS AND
METHOD FOR LIQUID CRYSTAL DISPLAY**

Customer No.: 30827

Confirmation No.: 7401

Art Unit: 2629

Examiner: Pham, Tammy T.

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Applicants request review of the Final Office Action dated April 4, 2011 for at least the reasons set forth below. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. Claims 1, 8-9, 11-12, 15-27 and 29-30 are currently pending, with claims 1 and 8 being identified as withdrawn. Applicants respectfully submit that there are clear errors in the rejections contained in the Final Office Action.

In the final Office Action, claims 9, 11-12, 15-27 and 29-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cairns et al. (“Cairns1”) (U.S. Publication No. 2002/0030653) in view of Cairns et al. (“Cairns2”) (U.S. Patent No. 6,268,841), Enami et al. (U.S. Patent No. 5,892,493), Morita (U.S. Patent No. 6,989,810), Nitta et al. (U.S. Patent No. 6,661,402) and Eto et al. (U.S. Patent No. 6,288,697).

A. Rejection of Claim 30 under 35 U.S.C. 103(a) over Cairns1 in view of Cairns2, Enami, Morita, Nitta and Eto is improper and should be reversed.

Claim 30 is allowable over the cited references in that claim 30 recites a combination of elements including, for example, “performing a time-division on a plurality of digital pixel data for a first horizontal period using a polarity control signal and an even/odd signal, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data; raising a voltage of the time-divided pixel data directly supplied from the positive and negative paths using a level shifter... outputting a common voltage Vcom to the corresponding data lines for a disable period of the input source output enable signal of the second horizontal period...” For the reasons set forth below, none of the cited references teaches or suggests at least these features of claim 30.

In the Final Office Action at pages 5 and 6, the Examiner admits that the main reference Cairns1 fails to disclose the aforementioned features of claim 30, and then cites Nitta to allegedly cure the deficient teachings of Cairns1.

First, the Examiner asserts at page 6 that “Nitta teaches of that the pixel data sequentially being outputted to positive and negative paths by unit of adjacent pixel data (Fig. 2) using a polarity control signal and an even/odd signal (Fig. 2, item 216).” However, as shown in Fig. 2 of Nitta, item 216 in Fig. 2 is a scan horizontal synchronizing signal that is applied to the scanning circuit 205. See also Nitta at 3:1-2. The scanning circuit 205 performs a line-sequential selection for the liquid crystal panel (see *id.* at 2:47-48) and thus does not relate to a modulation of pixel data. Also, it is unclear why the scan horizontal synchronizing signal of Nitta can be equated with both the polarity control signal and the even/odd signal as recited in claim 30.

Second, the Examiner also asserts at page 6 that Nitta discloses “raising a voltage of the time-divided pixel data (Fig. 2, items 228, 229) directly supplied from the positive and negative paths (Fig. 2, items 228, 229) using a level shifter (Fig. 2, item 231).” As recited in claim 30, the time-divided pixel data is a digital data in the claimed invention. However, assuming *arguedo* that the amplifier 231 in Nitta corresponds to a level shifter, the amplification is performed on analog signals output from the positive and negative DACs 228 and 229 as shown in Fig. 2 of Nitta. DAC stands for Digital to Analog Converter. Therefore, contrary to the Examiner’s assertion, Fig. 2 of Nitta fails to disclose the aforementioned features of claim 30.

Third, the Examiner asserts at page 6 that Fig. 2 of Nitta discloses “converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal and converting the other digital pixel of the adjacent digital pixel data inputted to the negative path into a negative pixel signal.” This feature of claim 30 is illustrated in Fig. 3 of the present application in which the DAC part 60 including PDAC and NDAC converts the digital pixel data provided by the positive and negative paths PCH and NCH to positive and negative pixel signals. As discussed above, the digital to analog conversion in the claimed invention occurs after the time-divided digital pixel data are level-shifted as recited in claim 30. However, as shown in Fig. 2, the amplification of Nitta is performed after the display data 207 is converted into analog signals by the positive and negative DACs 228 and 229. Therefore, contrary to the Examiner’s assertion, Fig. 2 of Nitta fails to disclose the aforementioned features of claim 30.

With respect to the common voltage Vcom in claim 30, the Examiner asserts at pages 3 and 4 that the teachings of Cairns1 still reads on this limitation referring to Paragraph [0061] and Fig. 1. Claim 30 requires that a common voltage Vcom be output to the corresponding data lines for a disable period of the input source output enable signal of the second horizontal period. First, as previously presented, the reference voltages of Cairns1 correspond to the reference gamma voltages in Figure 5 of the present application, which is different from the Vcom voltage of the claimed invention. Those of ordinary skill in the LCD art would appreciate that the term “Vcom” has a distinctive meaning for driving the liquid crystal panel, which is different from the references voltages used for digital to analog conversion in Cairns1. Second, the reference voltages in Cairns are supplied to the DACs 21, not to the data lines as required by claim 30. Also, it is unclear how the plurality of references voltages in Cairns, each having a different voltage level for digital to analog conversion, can be equated with a single voltage level of the Vcom voltage of the claimed invention.

For at least the foregoing reasons, the rejection of claim 30 under 35 U.S.C. 103(a) over Cairns1 in view of Cairns2, Enami, Morita, Nitta and Eto is improper and should be reversed.

B. Rejection of Claims 9 and claims 11, 12, 15-27 and 29 under 35 U.S.C. 103(a) over Cairns1 in view of Cairns2, Enami, Morita, Nitta and Eto is improper and should be reversed.

Claim 9 is allowable over the cited references in that claim 9 recites a combination of elements including, for example, “a multiplexer part performing a time-division on the digital pixel data for a plurality of data lines for a first horizontal period using a polarity control signal and an even/odd signal, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data; a level shifter part raising a voltage of the time-divided pixel data directly supplied from the positive and negative paths of the multiplexer part... outputting a common voltage Vcom to the corresponding data lines for a disable period of the source output enable signal...” For similar reasons as discussed with respect to claim 30, Applicants respectfully submit that none of the cited references teaches or suggests at least these features of claim 9, and claim 9 and claims 11, 12, 15-27 and 29, which depend from claim 9, are thus allowable over the cited references. Accordingly, rejection of claims 9 and claims 11, 12, 15-27 and 29 under 35 U.S.C. 103(a) over Cairns1 in view of Cairns2, Enami, Morita, Nitta and Eto is improper and should be reversed.

In light of the remarks noted above, Applicant respectfully submits that the pending claims are patentable over the prior art cited in the April 4, 2011 Final Office Action. Accordingly, Applicant respectfully requests that the Patent Office withdraw the rejections of the Final Office Action and issue a Notice of Allowance or a new, non-final Office Action.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911.

Dated: August 1, 2011

Respectfully submitted,

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